ETHERNET CHANNEL ESTIMATION DEVICE AND METHOD

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the technical field of channel estimation and, more particularly, to a Gigabit Ethernet channel estimation device and its estimation method.

2. Description of Related Art

For conventional communication system, Inter-symbol-interference (ISI) occurs if received signals on a receiving end are commonly affected due to the limited bandwidth of transmission channels. Accordingly, a Decision Feedback Equalizer (DFE) is used to eliminate ISI. The DFE includes a feedforward equalizer (FFE) and a feedback equalizer (FBE). However, for a receiver system of a Gigabit Ethernet as shown in Fig. 1, in addition to the channel impairment, the convergence of DFE, timing recovery, echo cancellation, and NEXT(Near End Cross Talk) loop cancellation are also required to be accomplished when receiving the signals. Thus, circuitry for DFE convergence, timing recovery, echo cancellation, and NEXT loop cancellation are set in the receiver system. In order to avoid system divergence caused by interaction of those circuitry, the conventional approach is to directly set the optimized coefficients for those circuitry in initialization for convergence. The optimized coefficients are determined through channel estimation.

CAT-5 cable is defined as a transmission medium in IEEE 802.3u and 802.3ab standards. The CAT-5 cable is a time-invariant channel, which

can be tested for obtaining the coefficients based on different transmission line-length in advance. For an MLT-3 transmission format applied to IEEE 802.3u (Fast Ethernet), the transmission line-length can be determined according to a received signal on a receiving end and accordingly applied to a mapping or conversion table to determine the coefficients. However, for a PAM-5 signal format used in a Gigabit Ethernet network, the transmission line-length cannot be estimated using the aforementioned methods. Additionally, the aforementioned methods have poor estimation accuracy in some circumstances (such as when the power of the transmitter is too high or too low). Another method of line-length estimation is to measure received signal energy. However, this method has the same disadvantages as compared with the others.

Since the CAT-5 channel is a kind of time-invariant environment, coefficients of a corresponding DFE or A/D auto-gain controller (AGC) can be determined if line-length can be accurately estimated.

The conventional method to estimate transmission line-length is through determining the relationship between the frequency spectrum of received signal and the transmission line-length. However, the low frequency response of received signal is greatly affected by transformer. Thus the variance of low frequency response of received signal is large with respect to different transformers manufactured by different manufacturers. Further, since most noise is present in the high frequency part, the variance of high frequency spectrum response of received signal is also large. Therefore, both the low and high frequency parts of received signal are not

suitable for line-length estimation. According to simulation, a ratio of frequency response of 6 and 43 MHz can be used for transmission line-length estimation. However, in practice, the cost for hardware implementation is very high due to a lot of multiplication and addition computations are required for executing discrete Fourier transform (DFT).

Therefore, it is desirable to provide an improved channel estimation device and method to mitigate and/or obviate the aforementioned problems.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an apparatus for communication channel estimation and an estimation method to accurately estimate channel(transmission line) length, such that coefficients of the DFE, A/D, and/or auto-gain controller can be obtained to generate stable and rapid convergence.

To achieve the objects, the apparatus for communication channel estimation device of the present invention includes: a frequency response square computing circuit, to generate a first frequency response corresponding to a first frequency and a second frequency response corresponding to a second frequency according to a input signal, and to square the first and the second frequency response; and an estimating circuit, to estimate a channel length according to the squares of the first frequency and the second frequency response. Wherein the input signal is transmitted in a symbol rate and the first frequency and the second frequency are 1/M and 1/N times of the symbol rate respectively, wherein M and N are in the order of 2.

Other objects, advantages, and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a conventional system architecture of a Gigabit Ethernet receiver;

FIG. 2 shows a system architecture of an Ethernet channel estimation device according to the embodiment of the present invention;

FIG. 3 shows a frequency response of an input signal;

FIG. 4 is a schematic diagram of a frequency response square computing circuit according to the embodiment of the present invention;

FIG. 5 is a schematic diagram of a magnitude automatic aligning and adjusting circuit according to the embodiment of the present invention;

FIG. 6 is a diagram of pseudo codes of FIG. 5 according to the embodiment of the present invention;

FIG. 7 is a diagram of a ratio comparing circuit according to the embodiment of the present invention;

FIG. 8 is a diagram of a ratio mapping circuit according to the embodiment of the present invention; and

FIG. 9 is a flowchart of an Ethernet channel estimation method according to the embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 2 illustrates a system architecture of an Ethernet channel estimation device according to the embodiment of the present invention. As

shown, the device includes a frequency response square computing circuit 10, a magnitude automatic aligning and adjusting circuit 20, a ratio comparing circuit 30 and a ratio mapping circuit 40.

For the Gigabit Ethernet, of which the symbol rate is 125 MHz, the frequency response square computing circuit 10 generates frequency responses of a first frequency at 15.625 MHz (125/8 MHz) and a second frequency at 31.25 MHz (125/4 MHz) respectively, and squares the magnitudes of frequency responses at the first frequency and the second frequency respectively. The magnitude automatic aligning and adjusting circuit 20 normalizes the square magnitudes of frequency response to generate a ratio of a first window signal to a second window signal. The ratio comparing circuit 30 multiplies the second window signal by a current ratio and compares the result with the first window signal to determine whether the current ratio is too large or too small. When the number of comparison indicating that the current ratio is too large or too small exceeds a predetermined number, a comparing result is output from the ratio comparing circuit. The ratio mapping circuit 40 adjusts coefficients of a DFE, an analog AGC or a digital AGC according to the comparing result.

In the conventional method, a ratio of 6 and 43 MHz frequency responses is selected to estimate line-length. As shown in FIG. 3, the frequency response square computing circuit 10 select 8 point for computing frequency response lf at the first frequency (15.625 MHz) and 4 point for computing frequency response hf at the second frequency (31.25 MHz), wherein 8-point DFT of the input signal at the first frequency and

4-point DFT of the input signal at the second frequency are represented by the following equations (1) and (2).

$$lf\,|_{15.625MHz} = \sum_{n=0}^{7} x(n)e^{-\frac{j2\pi n}{8}} = (x(0)-x(4)) - j(x(2)-x(6)) +$$

$$\frac{1}{\sqrt{2}}x(1)(1-j)) + \frac{1}{\sqrt{2}}x(3)(-1-j) + \frac{1}{\sqrt{2}}x(5)(-1+j) + \frac{1}{\sqrt{2}}x(7)(1+j)...(1)$$

$$hf\,|_{31.25MHz} = \sum_{n=0}^{3} x(n)e^{-\frac{j2\pi n}{4}} = (x(0)-x(2)) - j(x(1)-x(3))..... (2)$$

Because the factor of $\frac{1}{\sqrt{2}}$ in the equation (1) is not easy to be implemented by hardware, the factor of $\frac{1}{\sqrt{2}}$ is replaced with +1 and thus the equation (1) becomes:

$$lf\,|_{15.625MHz} = \sum_{n=0}^{7} x(n)e^{-\frac{j2\pi n}{8}} \approx (x(0)+x(1)-x(3)-x(4)-x(5)+x(7)) -$$

$$j(x(1)+x(2)+x(3)-x(5)-x(6)-x(7))..... (3)$$

As such, the square of first frequency response magnitude is pow_lf which is equal to $[x(0)-x(3)+x(1)-x(4)+x(7)-x(5)]^2 + [x(1)+x(2)+x(3)-x(5)-x(6)-x(7)]^2$, and the square of second frequency response magnitude is pow_hf which is equal to $[x(0)-x(2)]^2 + [x(1)-x(3)]^2$.

FIG. 4 shows a diagram of the frequency response square computing

circuit 10 in detail. The circuit 10 essentially computes the square of frequency response magnitude of an input signal at the first frequency and the second frequency. The circuit 10 includes a plurality of adders, a plurality of multipliers and a plurality of delay elements. When the circuit 10 receives the input signal, it generates the square of first frequency response magnitude, i.e., pow_lf = $[x(0)-x(3)+x(1)-x(4)+x(7)-x(5)]^2+$ $[x(1)+x(2)+x(3)-x(5)-x(6)-x(7)]^2$, and the square of second frequency response magnitude, i.e., pow_hf = $[x(0)-x(2)]^2 + [x(1)-x(3)]^2$.

The two signals pow_lf and pow_hf are greater than or equal to 0 and increasing. When the two signals are accumulated over allowable hardware word-length, the ratio of the two signals is in error due to overflow. To overcome this, when the circuit 20 finds that the accumulation of the two signals is over a specific value (i.e. $0X8000_H$), the circuit 20 keeps to generate a first window signal win_lf and a second window signal win_hf in normalization after, for example as shown in FIG. 5, the upper bits of pow_lf or pow_hf are shifted right 8 bits and then filled with 0. The circuit 20 can be implemented by pseudo codes in FIG. 6 through hardware description languages such as Verilog or VHDL.

Therefore, the ratio of line-length estimation is:

$$ratio = \frac{|l_f|_{15.625MHz}|^2}{|hf|_{31.25MHz}|^2} = \frac{pow\_lf_{15.625MHz}}{pow\_hf_{31.25MHz}} = \frac{win\_lf}{win\_hf} \quad .....(4)$$

As shown in FIG. 7, the ratio comparing circuit 30 with reduced hardware area includes a comparator 32, a first multiplier 31, a first adder

33 and appropriate logic circuits for executing the dividing operation. After initialization, an initial ratio value "ratio_i" of a channel with 0 meter is loaded by a signal "load" to a register as a current ratio. The first multiplier 31 multiplies the second window signal "win_hf" by the current ratio to produce a result. The comparator 32 compares the result and the signal "win_lf" to determine whether the current ratio is too large or too small. The first adder 33 accumulates the result from the comparator 32 so that when the number of too large or too small current ratio is over a predetermined number such as two, the current ratio is adjusted, wherein u is step size of ratio. When a signal "cnt[1] " is "0", it indicates that the accumulated number of the signal "win_lf" larger than the signal "win_hf" is over two times; i.e., the current ratio is determined to be too large for two times. Thus, the current ratio is reduced by the scale of –u. Conversely, when the signal "cnt[1] " is "1", the current ratio is increased by the scale of +u.

As shown in FIG. 8, the ratio mapping circuit 40 includes a second multiplexer 41, a second multiplier 42 and a third adder 43. After initialization, an initial coefficient value "dagc_i_r" of digital AGC is loaded by the signal "load" to a register. The second multiplexer 41 has a first input terminal to input a constant +1, a second input terminal to input a constant –1, and a control terminal connected to the signal "cnt[1] " from the first adder 33 such that the constant +1 or –1 is output to adjust coefficients of the digital AGC when the first adder 33 is accumulated over a predetermined number such as two times. The second multiplier 42

multiplies the output of the second multiplexer 41 by a specific constant. The third adder 43 accumulatively adds the coefficient of the digital AGC and the output of the second multiplier 42 to adjust the coefficient of the digital AGC. A specific constant "delta_g" is defined as a ratio of a digital AGC's coefficient value to a line-length ratio value multiplied by the step size u under different channel lengths. For example, if the line-length ratio is increased linearly from 3.0 (ratio_i) to 4.125 as a channel length changes from 0 m to 100 m, and the digital AGC is increased linearly from 8.0 (dagc_I_r) to 25.0, while the line-length ratio is converged with u speed, the digital AGC is converged by the speed of "delta_g", wherein delta_g = u * (slope2/slope1), slope1 = (4.125-3.0)/100 and slope2 = (25.0-8.0)/100.

FIG. 9 shows a flowchart of the Ethernet channel estimation method disclosed in the embodiment of the present invention. In step S301, an input signal is inputted. In step S302 (step for computing the square of a first frequency response), instead of the computing the square of prior frequency response at 6 MHz, the square of "pow_lf" of 8-point first frequency response for the input signal at the first frequency (15.625 MHz) is computed by the equation $[x(0)-x(3)+x(1)-x(4)+x(7)-x(5)]^2$ + $[x(1)+x(2)+x(3)-x(5)-x(6)-x(7)]^2$. In step S303 (step for computing the square of a second frequency response), instead of computing the square of prior frequency response at 43 MHz, the square of "pow_hf" of 4-point second frequency response for the input signal at the second frequency (31.25 MHz) is computed by the equation $[x(0)-x(2)]^2 + [x(1)-x(3)]^2$.

In step S304 (normalizing step), the normalization is performed

when "pow_lf" or "pow_hf" is accumulated to overflow. This is because both "pow_lf" and "pow_hf" greater than or equal to 0 are increased as a ratio of "pow_lf" to "pow_hf" is computed for line-length estimation. In this case, the ratio of "pow_lf" to "pow_hf" is an error value. Therefore, the normalizing step divides the signal "pow_lf" or "pow_hf" by a specific value (256) when the accumulation of "pow_lf" or "pow_hf" is over a specific value ($0X8000_H$) to generate a first window signal "win_lf" and a second window signal "win_hf" in normalization. Thus, the error ratio caused by the overflow is eliminated.

In step S305 (ratio computing step), it receives the first window signal and the second window signal computed by step S304 and computes the ratio, wherein the ratio and the channel length have a relation approximate to linearity. Thus, the ratio can be converted into coefficients corresponding to the DFE, analog or digital AGC.

As aforementioned, the Ethernet channel estimation device and method uses a line-length estimation method regardless of transmitter power and thus has high accuracy. Additionally, the approximate DFT computation is used in the invention and the prior divider is replaced with the simple logic circuits and comparators to simplify required hardware. In such a simple configuration, the present invention provides accurate conversion to coefficients of the DFE, analog or digital AGC.

Although the present invention has been explained in relation to its preferred embodiment, it is to be understood that many other possible modifications and variations can be made without departing from the spirit

and scope of the invention as hereinafter claimed.